Resistive Switching in High-Density Nanodevices Fabricated by Block Copolymer Self-Assembly

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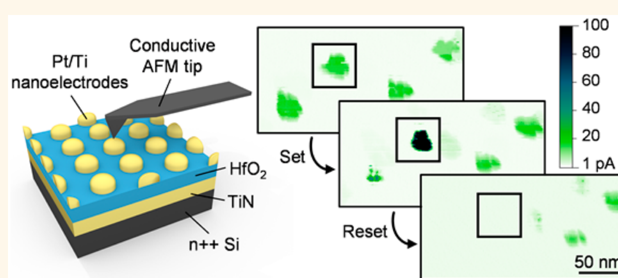
ABSTRACT Bipolar resistive switching memories based on metal oxides offer a great potential in terms of simple process integration, memory performance, and scalability. In view of ultrahigh density memory applications, a reduced device size is not the only requirement, as the distance between different devices is a key parameter. By exploiting a bottom-up fabrication approach based on block copolymer self-assembling, we obtained the parallel production of bilayer Pt/Ti top electrodes arranged in periodic arrays over the HfO_2/TiN surface, building memory devices with a diameter of 28 nm and a density of 5×10^{10} devices/cm^2. For an electrical characterization, the sharp conducting tip of an atomic force microscope was adopted for a selective addressing of the nanodevices. The presence of devices showing high conductance in the initial state was directly connected with scattered leakage current paths in the bare oxide film, while with bipolar voltage operations we obtained reversible set/reset transitions irrespective of the conductance variability in the initial state. Finally, we disclosed a scalability limit for ultrahigh density memory arrays based on continuous HfO_2 thin films, in which a cross-talk between distinct nanodevices can occur during both set and reset transitions.



KEYWORDS: resistive switching · ReRAM · high density · HfO_2 · bottom-up fabrication · block copolymer · self-assembly

Bottom-up nanofabrication approaches based on block copolymer (BCP) self-assembly offer the possibility to generate high-density features at nanoscale.[1,2] This key-enabling technology provides a simple and powerful instrument to fabricate high-density arrays of nanostructured resistive switching (RS) devices. Indeed, resistive switching memories (ReRAM) are among the main candidates for future solid-state memory applications able to satisfy the increasing demands in terms of data storage capacity, low power consumption, and fast accessing time.[3−5] RS devices consist of two terminals capacitor-like structures in which the electrical resistance of the system can be reversibly switched between two (or more) nonvolatile values.[6] In a variety of materials, the RS mechanism can be explained in terms of formation of a filamentary conductive path bridging the two electrodes in the low resistance state (LRS) during the set operation, while in the reset process the filament is partially disrupted, leading to the high resistance state (HRS).[7,8] Usually, the switching is initiated by a unique forming process which is responsible for the first establishment of the conductive filament. Because of the small filament size, filament-based RS memories are particularly suited for scaling. In particular, transition metal oxides are among the main candidates as dielectric materials in future RS memories.[9] HfO_2 is increasingly becoming a model example, since it offers excellent CMOS process integration capability and promising memory performances.[10,11] Recent reports revealed sub-10 nm conductive channel diameter in HfO_2-based RS devices[12,13] and well-functioning nanoscale devices have been fabricated using either electron beam lithography or a three-dimensional stacking procedure.[14−16] However, these fabrication methods allow the definition of a limited number of memory cells, while the scalability limit of high-density packing has not been explored.

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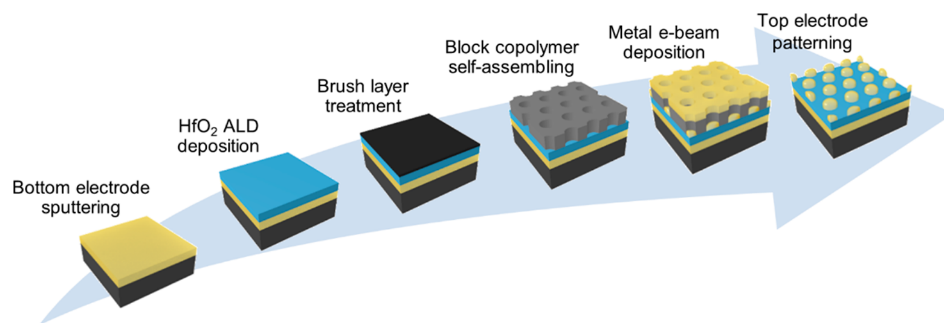

Figure 1. Procedure for the top electrode patterning. A BCP self-assembled template was adopted for pattern transfer with a lift-off process.

In this view, BCP thin films demonstrated the ability to self-assemble in periodic nanodomains that can be exploited for the fabrication of nanoscale features, often in combination with current top-down patterning technologies.[1,17,18] This high throughput patterning technique offers the advantage of producing ultrahigh density devices, yet maintaining a good control over the device size and spacing as a function of the polymer molecular weight.[19−21] BCPs allow the definition of regular patterns with dimension and spacing that easily go beyond the limits of current optical lithography,[22,23] and have been used for the formation of complex patterns in different applications such as FinFET transistors, circuit interconnects, capacitors, and charge trapping memories.[24−26] BCPs have also been employed in the fabrication of phase change memories for a reduction of the electrode contact area, achieving a significant power reduction.[27] RS device top electrode downscaling using BCP in combination with electron beam lithography has been reported, in which the BCP was applied to define narrow but isolated features.[28]

In this work, we employ a BCP-assisted lithographic process for the parallel fabrication of nanosized, high-density metal electrodes organized in regular arrays over the HfO_2 switching material. To the best of our knowledge, the block copolymer self-assembly strategy we used allows producing the most dense array of ReRAM devices that has been reported in the literature so far. With the conductive tip of an atomic force microscope (C-AFM), we achieve a selective addressing of the single nanodevices, in order to obtain the switching phenomenon at the nanoscale and investigate the effect of density upscaling on the system properties. This work aims to provide a missing piece of information that is fundamental to assess the effective scalability of ReRAM devices in high-density arrays showing original and counterintuitive electric phenomena that have not been identified yet.

RESULTS AND DISCUSSION

Fabrication of Nanoscale RS Devices with BCP Template. Figure 1 summarizes the adopted process workflow to obtain an ordered array of RS devices by BCP lithography. The first step consists in the sputter deposition of the TiN bottom electrode, followed by the atomic layer deposition (ALD) of a 3 nm thick HfO_2 film and finally by the Pt/Ti top electrode nanopatterning. This final step employs a lift-off process with a nanoporous template formed by BCP self-assembling.[19,20,29,30]

Before BCP deposition, the oxide surface was functionalized with a brush layer of P(S-*r*-MMA) random copolymer, which is necessary in order to modify the poly(methyl methacrylate) (PMMA) preferential wetting of the surface and obtain a perpendicular orientation of the cylindrical nanodomains in the above BCP layer.[29,30]

The BCP phase separation was induced with a rapid thermal processing (RTP) heat treatment that allowed a short processing time of 5 min.[23,31] We employed a PS-*b*-PMMA block copolymer with PS content of 70%, obtaining PMMA cylindrical nanodomains with hexagonal periodic distribution within the polystyrene (PS) matrix. Upon selective removal of the PMMA polymeric component, a nanoporous PS periodic structure was obtained, as shown in the SEM image of Figure 2a. The BCP lithographic technique offers the possibility of a fine-tuning of the device size and spacing as a function of the polymer molecular weight (M_w).[21] By employing a M_w of 102 kg/mol, we obtained devices with a diameter of 28 $\pm$ 1 nm and a center-to-center distance of 47 $\pm$ 1 nm, which resulted in an average spacing between neighboring devices of 19 $\pm$ 1 nm and a density of 5 $\times$ 10^{10} devices/cm^2. The Pt/Ti top electrode was electron-beam deposited through the nanoporous template, and a solvent-assisted lift-off process was adopted to produce the ordered arrays of nanopatterned top electrodes shown in the SEM image of Figure 2b. In this step, we deposited a bilayer structure composed of 4 nm Ti and 6 nm Pt, obtaining the final device structure descripted in Figure 2c. The Ti layer was chosen because of its oxygen-reacting property, which was demonstrated to significantly reduce the forming voltage and the device variability.[34,35] Figure 2d shows the sample surface morphology obtained by AFM, where distinct nanodevices with hexagonal distribution are clearly distinguishable.

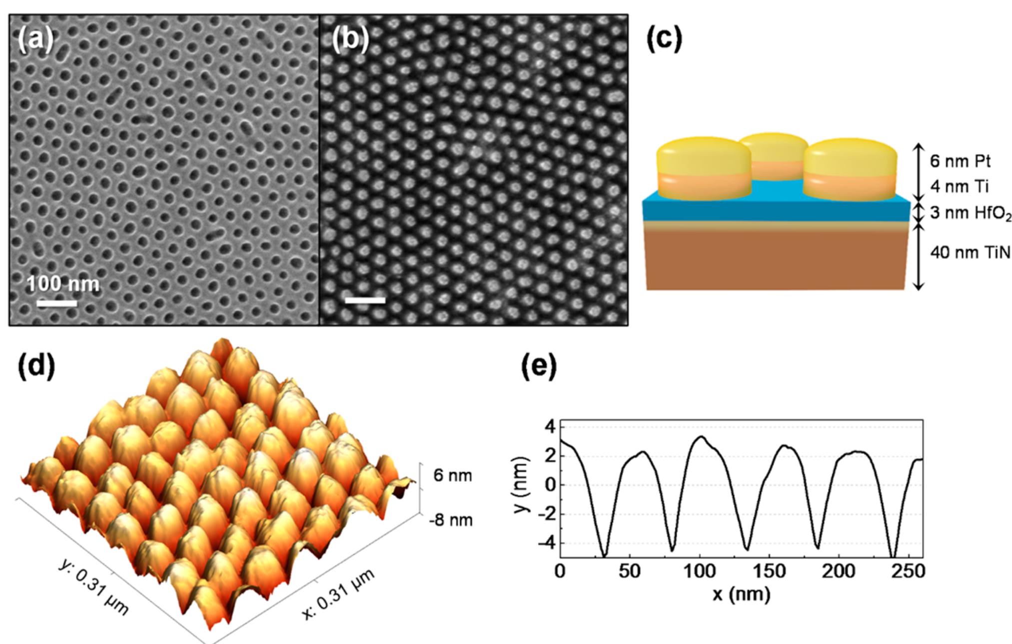

Figure 2. SEM plane views of (a) nanoporous PS template obtained by BCP self-assembling in periodic perpendicular cylinders and (b) arrays of Pt/Ti top electrodes on top of the HfO_2 surface obtained from the self-assembled polymeric template depicted in (a). (c) Device stack representation. (d) AFM surface morphology acquired with a Pt/Ir-coated tip showing the top electrodes with hexagonal distribution and relative line scan (e) displaying the electrodes height.

In Figure 2e, a line scan extracted from Figure 2d is shown. The average electrode height of 8 ± 1 nm obtained from AFM data analysis is compatible with the deposited metal thickness, while the electrode size appears larger than in the SEM image (Figure 2b) because of the lateral convolution with the AFM tip geometry.

Because of the oxidation of the TiN upper interface prior to the HfO_2 deposition, an additional oxide layer of roughly 2 nm of mixed TiO_2 and TiO_xN_y components was found by XPS analysis (data not shown). This additional layer was reported to increase the LRS resistance, which is desirable for large array memory architectures.[15] This highly defective interface can additionally accommodate excess oxygen species during the set process, serving as oxygen reservoir for the filament oxidation in the subsequent reset process.[32] Besides, the deposition of a thin 3 nm HfO_2 was chosen in order to lower the operation voltages, as required for RS device scaling.[33,34]

Initial State Characterization of the Nanoscale RS Devices. Figures 3a and 3b display simultaneously acquired C-AFM topographic and current maps for the characterization of the initial leakage conductance of the devices. A potential difference of 1.5 V was chosen to highlight the device variability, yet low enough to avoid electric field-induced perturbations, as verified with repeated scans. A close correlation can be found between the hexagonally packed Pt/Ti metal electrodes in Figure 3a and the uniform conductive spots in Figure 3b, confirming the equipotential behavior of the nanometer-sized metal electrodes, which is the first requirement for their correct operation. We noticed however very different leakage current levels among different devices. By plotting the cumulative distribution of the initial state resistances, two different conditions can be defined in Figure 3c. High resistance devices, which cover nearly 80% of the total population, show a low dispersion, while the remaining low resistance devices have a conductance value spread over almost 2 decades. Repeating the initial state analysis in a different area of the sample and with a different voltage, the same general trend was obtained (Figure S1, Supporting Information).

In order to investigate the device initial state variability, we assessed the oxide nonhomogeneity at the nanoscale by acquiring current maps of the bare HfO_2/TiN film surface, before top electrode patterning, using the C-AFM tip as top electrode (Figure 4). The majority of the HfO_2 film presents a very low leakage current, while isolated current spots indicate the presence of randomly spread leaky sites, with a current level that differs greatly between the different sites.[35] The highly insulating background correlates well with the 80% of highly resistive devices reported in Figure 3, while the leaky sites, which show a wide current dispersion, are likely responsible of the resistance variability over 2 decades for the 20% of the most conductive nanodevices. This C-AFM electrical characterization of the bare oxide is in agreement with what is in general observed for amorphous 3 nm HfO_2 samples deposited on TiN, with no evident correlation between the surface morphology and the location of the leaky sites.[36,37] It is worth noting that the same general

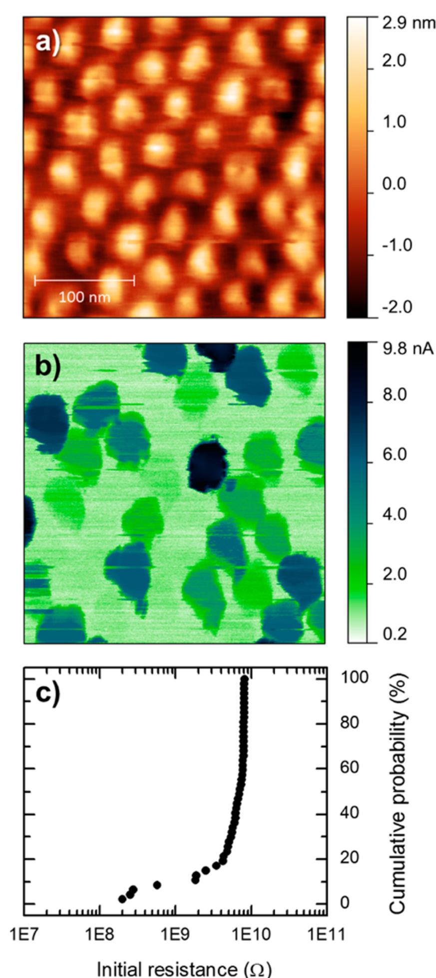

Figure 3. AFM morphology (a) and corresponding current map (b) of top metal electrodes defined by BCP lithography on the HfO_2 surface, acquired with an applied bias of 1.5 V. Because of the large curvature radius of the diamond-coated AFM tip used, the metal electrodes appear connected in the current map and the z scale of the morphology map underestimates the real electrodes height. (c) Initial state resistance distribution of the devices in figure (b).

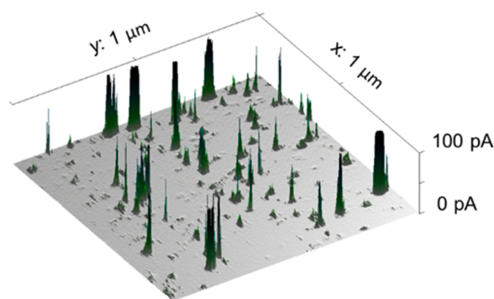

Figure 4. C-AFM current map of a 3 nm HfO_2/TiN bare surface acquired at 1.5 V bias displaying the film nanoscale conductance variability.

behavior is also observed in HfO_2 films grown on different substrates irrespective of the specific substrate composition and morphology, suggesting that the conductance inhomogeneity is rather an intrinsic property of the HfO_2 film.[38] We observed an average number of 100 spots/μm^2 at 1.5 V, a value in agreement with previous observations.[36] Comparing this value with the density of 500 devices/μm^2 in the sample with BCP patterned electrodes, we can clearly correlate the 20% of highly conductive devices with the inherent presence of leakage current paths in the bare HfO_2/TiN stack. This relation is illustrated in Figure S2 with an overlay of the AFM current map with a SEM plane view showing the patterned nanodevices with the same lateral scale.

Nanoscale Device RS Operations. With the sharp conductive tip of the C-AFM, we selectively addressed the individual nanoscaled memory cells. By placing the tip over a selected electrode and ramping the voltage, the forming transition can be obtained (Figure 5a). We repeated the operation on different randomly selected devices, finding forming voltages comprised in the 4.5−5.5 V range. This transition can be obtained regardless of the device initial resistance status, meaning that the inherent presence of leakage conduction paths is not a prerequisite for the device forming. When using a direct C-AFM tip contact (Pt−Ir coated tip as top electrode), previous works on 3 nm HfO_2 amorphous films point out that quite a high voltage (>16 V) is necessary to induce the oxide breakdown.[36,37] Indeed, acquiring voltage scans over the bare HfO_2/TiN surface in 25 random positions, no forming transition in the 0−10 V range was obtained, locating the tip in areas showing either leaky sites or low initial conduction (see Figure S3). In comparison with a direct C-AFM tip contact, the nanoscale electrical characterization of the RS system using nanoelectrodes defined by BCP lithography brings the big advantage that real devices are investigated. In this way, various artifacts located at the tip−oxide interface can be avoided (water meniscus, anodic oxidation, *etc.*),[39] while the device area can be carefully defined by the BCP template and the electrode material can be more easily selected. In this respect, the insertion of the Ti interlayer in the top electrode stack allowed to reproduce a memory stack widely adopted in the literature, since it was previously associated with a visible reduction of the forming voltage.[40−42]

Considering devices located in correspondence of leaky sites, their higher initial conductance can be manipulated with bipolar voltage operations. In Figure 5b, a current map acquired at 0.5 V shows in the scanned area two devices with high initial conductance. Selecting the device indicated by an arrow and performing a steady state negative voltage sweep (inset of Figure 5b), the device conductance is suppressed, as it is evident in the subsequent reading current map of the same area (Figure 5c). This can be interpreted as the reset of a device that is initially in a LRS, with the conductive channel already in place without the requirement of an initial forming step.

Because of the small electrode dimension, which is of the same order of magnitude of the tip contact area,

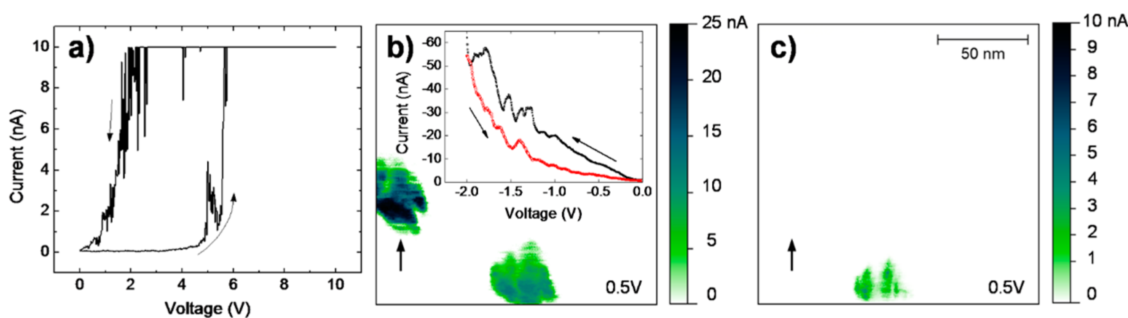

Figure 5. (a) High initial resistance device: Forming process in a Pt/Ti/HfO_2/TiN nanodevice. 10 nA is the maximum detectable current. (b,c) Initially leaky devices: current maps acquired at 0.5 V before and after the reset operation (inset) of the device indicated by the arrow. After reset, this device is not visible anymore in the reading current map (c).

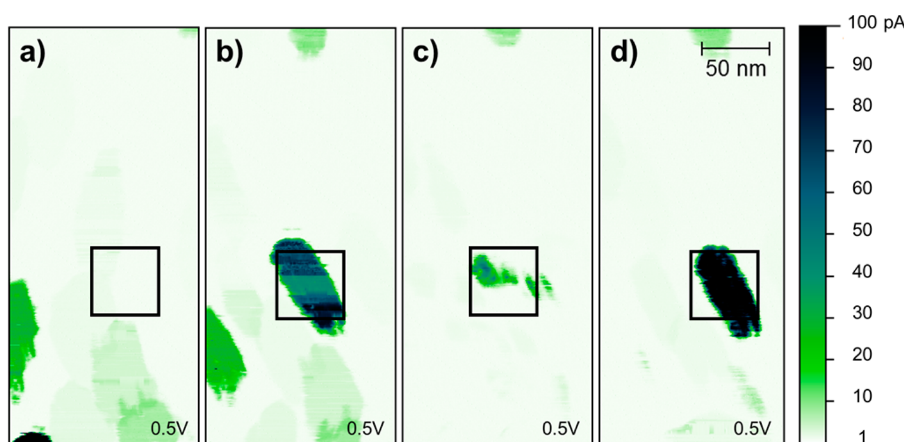

Figure 6. Current maps (0.5 V bias) acquired before the switching processes (a), after the set process with +4 V (b), after reset with −3 V (c), and after set with +4 V (d). The black square, containing a single nanodevice, encloses the area where the tip was scanned with +4 V/-3 V to induce the set/reset transitions. The elongated shape of the metal electrodes is an artifact caused by a drift in the scanning system.

a different C-AFM procedure was developed to gain better reproducibility during repeated set/reset processes. By scanning the tip over only one selected device with a constant applied bias, we improved the tip−electrode contact, while the applied bias was chosen high enough to induce the RS phenomenon. The induced conductance modification was then inspected with a following reading current map over a larger area at a low nonperturbing voltage.

The result of this switching procedure is reported in the series of reading current maps of Figure 6. In Figure 6a, a current map displays the initial resistance status of the devices. The C-AFM tip was then scanned with a constant bias of +4 V over the area enclosed by the black square (50 nm side), containing a single device which exhibits an initial current level below the ammeter sensitivity but was visible in the related topographic map (not shown). The subsequent current map of the whole area (Figure 6b) shows a significant conductance increase of the device under test (forming process). The voltage required to induce the forming transition was is in this case slightly lower than that required for punctual C-AFM tip operations as in Figure 5a, thanks to the longer lasting voltage stress induced with scanning tip operations, along with a more stable tip−electrode contact that helps reducing the contact series resistance. Scanning again over the same device with −3 V, we substantially suppressed the conductivity (reset), as visible in Figure 6c, while with the application of +4 V we were able to restore the low resistance state (Figure 6d). It is worth noting that the reading current maps were acquired about 10 min after the switching occurred, indicating a nonvolatile switching in resistance.

The same operation was also performed in the series of current maps reported in Figure 7 on a device that exhibited a not negligible initial state leakage current, as evident in Figure 7a. However, we noted that after the application of +4 V to the area enclosed by the black square, in Figure 7b we were able to increase the device conductivity to a level comparable with the one of the device selected in Figures 6b and 6d, regardless of the initial device variability. Moreover, by applying −4.5 V, we were able to annihilate the conduction path and reach a resistance value lower than that of the initial state, with a final current value under the detection limit (Figure 7c). The complete reset highlights the high control on the HRS that can be attained with nanosize devices, which is at the basis of the ON/OFF window opening previously observed in nanoscale systems.[34]

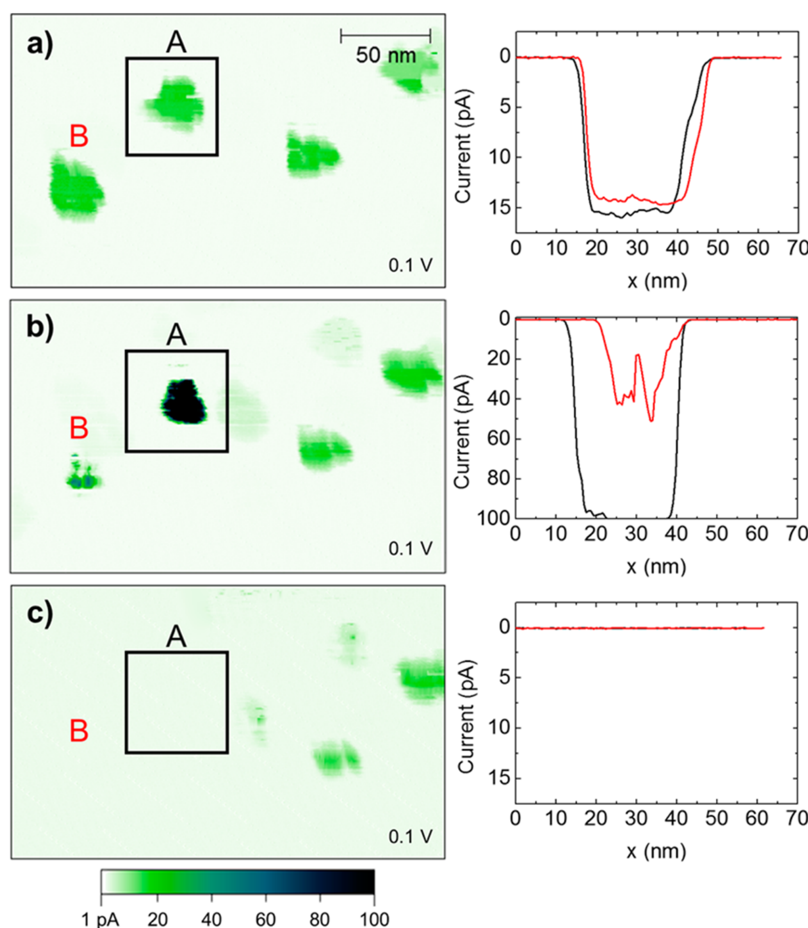

Figure 7. Current maps (0.1 V bias) acquired before the bipolar voltage operation (a), after set (b), and after complete reset (c). To induce the set and reset processes, the tip was scanned in the area enclosed by the black squares with a constant applied bias of +4 V (set) and −4.5 V (reset). On the right, line scans of the device to which the bias was applied (A, in black) and of the other correlated device (B, in red).

In Figure 7, another interesting aspect is visualized. The two conductive devices on the left side of Figure 7a (labeled A, in black and B, in red) share the same initial current value of 15 pA. After the application of a potential difference to the device enclosed by the black square (A), the not selected device at the bottom left (B) was also influenced. This cross-talk effect between distinct devices at a distance of 75 nm was obtained again during the reset operation, when both devices reached a resistance value higher than the initial state. It is worth noting that devices A and B are not nearest neighbors, otherwise they would appear contiguous as in Figure 3b. Additionally, the pitch is fully compatible with the presence of an additional electrode in between the two nanodevices. Nearest neighboring devices were unaffected during both set and reset operations, demonstrating that the observed cross-talk cannot be ascribed to the tip contacting many devices at the same time. Two other devices visible in Figure 7 at a distance of 80 and 130 nm were also unaffected, while a slight lowering in their conductance from Figure 7a to Figure 7c can be ascribed to the tip coating wearing out.

A similar cross-talk phenomenon was previously reported in the bare HfO_2/TiN stack using the conducting C-AFM tip as a mobile top electrode scanning the surface. After forming, distinct conductive spots appeared in the scanned region, while the afterward reset of one spot influenced the neighboring ones. The observed phenomenon was explained with the formation of bunches of connected conductive filaments during forming.[35] In the present case, we adopted an array of fixed devices instead of a mobile scanning electrode, with the C-AFM tip contacting only one device during forming. The presence of connected filaments should therefore be intrinsic of the HfO_2/TiN stack, as also indicated by the reinforcement of both devices after forming in Figure 7b.

Cross-Talk Mechanism. The mechanism behind this unexpected cross-talk effect deserves further considerations in order to achieve a plausible description of the physics of the system during the set/reset operations. Thermal profile simulations recently pointed out the thermal cross-talk, rather than the filament size itself, to be the ultimate limit for device scaling.[43] However, in our system, we can exclude thermal

cross-talk to be the cause of the linked switching behavior. Indeed, a second neighboring device was affected, while no nearest neighbors were influenced. Additionally, the cross-talk phenomenon is observed even during the set transition, which is mostly electric field-induced and can not be effectively driven by a pure thermal process. Furthermore, in a homogeneous dielectric medium the stray electric field does not extend much beyond the contacted electrodes and consequently a mere effect of the stray electric field isotropically extending out of the device A volume is not reasonable. Moreover, in this hypothesis also the first neighboring cells would be affected by the stray electric field during switching operations.

The experimental evidence indicates that the cells A and B are characterized by a similar leaky conduction through the oxide in the initial state (Figure 7a), and therefore they are already connected to the underlying TiN electrode, *i.e.*, an electrical circuit is already in place in the dielectric film. Furthermore, since the set and reset processes operated on device A lead to a conductance increase/decrease also of the unselected device B, the two devices are likely to share a common portion of the filamentary conduction paths, which is modified during set and reset operations and is responsible for the cross-talk effect.

The physical origin of the observed connection among distinct nanodevices, and the localization of the connected filamentary paths, should be sought in the structure and morphology of the insulating stack where the resistance switching occurs. Brivio *et al.*[35] suggested that the origin of the localized conduction paths can be located at the highly defective HfO_2/TiN interface, in which the TiN morphology and its oxidation behavior are also likely to play a role. In this respect, it is worth discussing our system in more detail. The bottom TiN electrode is composed of columnar crystalline grains extending throughout the film thickness, as evidenced by the AFM surface morphology and corroborated by the SEM cross sectional image reported in Figure 8. The height−height correlation function (HHCF) extracted from the AFM maps, which gives an estimation of the average grain dimension, returns a value of 17.4 ± 0.7 nm. Yet, grains with lateral size up to 40 nm are clearly visible in both the AFM and SEM data. The surface root-mean-square roughness (R_{RMS}) is equal to 1.57 ± 0.04 nm. This value is slightly lowered to 1.46 ± 0.08 nm upon exposure to 300 °C in air. These conditions are representative of the ambient experienced by the sample when it is introduced in the ALD chamber for the growth of the HfO_2 film. In particular, the smoothing of the TiN film upon air exposure is related to the oxidation of the TiN surface that results in the formation of a thin TiO_x layer. The oxidation behavior is reported to follow a logarithmic growth law which rapidly reaches the saturation thickness, with the vertical columnar boundaries acting

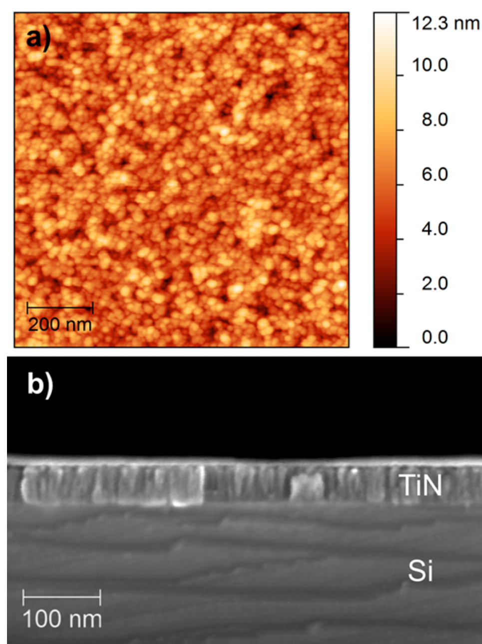

Figure 8. (a) Morphological characterization of the TiN surface performed upon oxidation in air by AFM operating in tapping mode. (b) SEM cross section of the HfO_2/TiN/Ti/Si stack. The TiN grains extend throughout the film thickness.

as fast diffusion paths for the oxygen species.[44,45] According to XPS analysis, a TiO_2 oxide film of 2−3 nm is formed, and the presence of a TiO_xN_y component was evidenced as well. As a result of this oxidation process, an HfO_2/TiO_x bilayer oxide is formed on top of the TiN electrode. It is interesting to note that the HfO_2 deposition performed by ALD forms an amorphous and uniform film conformal to the underlying surface. Conversely, the morphological and chemical structure of the TiO_x layer is strongly influenced by the TiN nanocrystalline structure. To summarize, the dielectric stack where the resistance switching takes place is composed of a nonhomogeneous dielectric with leaky paths that are already present in the initial state (Figure 4), and a defective TiO_x layer at the interface between the HfO_2 layer and the TiN bottom electrode.

Regarding the HfO_2/top electrode interface, it is worth to mention that the Ti layer inserted in the Pt/Ti top electrode is reported to lower the V_O formation energy in the HfO_2 film.[46] However, according to Clima *et al.*,[51] for the gettering layer thickness used in this work (4 nm), we can exclude the establishment of an asymmetric V_O profile or a V_O reservoir next to the top electrode in the HfO_2 film. Indeed, for thick (~10 nm) gettering layers, the observed switching polarity is opposite to the one observed in the present case. Apart from this, the Ti interlayer is expected also to act as an oxygen diffusion barrier, limiting oxygen outer diffusion through the Pt top electrode during the switching operation,[47] and to improve the Pt electrode adhesion, which is required for repeated AFM tip scans. However,

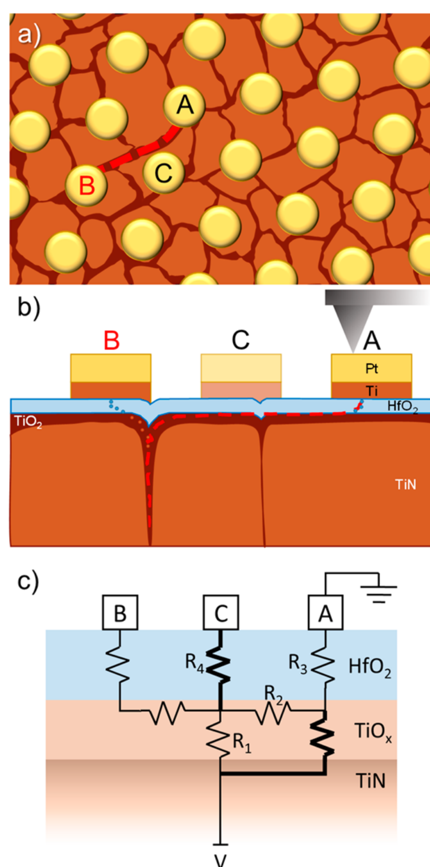

Figure 9. Pictorial view of the correlated switching for two different devices. On the top (a) a plane view shows the periodically patterned electrodes on top of the structured bottom electrode. (b) Cross section representing the current path along the grain boundaries. (c) Electrical schematic diagram illustrating the resistance network responsible for the cross-talk between devices A and B. The thin-line resistors correspond to low resistance paths, while the thick-line resistors are representative of a much higher resistance.

we can exclude a role of the top electrode and of its interface with the HfO_2 film in the cross talk mechanism due to its limited lateral extension.

On the basis of this detailed structural/compositional analysis of the nanodevices reported above, Figure 9 provides a pictorial view illustrating the structure of the system and the corresponding electrical diagram to elucidate the physical model accounting for the observed phenomena.

Electrodes A and B, which exhibit a cross-talk phenomenon as shown in Figure 7, are placed in correspondence of low resistance paths (thin-line resistors), while electrode C exhibits a much higher resistance (thick-line resistor), due to the nanoscale nonhomogeneity of the HfO_2 film. Further, taking into account also the discussed nonhomogeneity of the interfacial TiO_x dielectric layer, electrodes A and B are connected to the common TiN bottom electrode through a network of resistors that follow the lowest resistance paths and share a common portion of the path, depicted as R_1.

During the set operation, when a positive potential difference is applied between the bottom electrode and the electrode A, a filament reinforcement takes place in the HfO_2/TiO_x stack.[48,49] At the beginning, most of the voltage is dropping across the highly insulating HfO_2 layer, where V_O^{q+} are formed preferentially along the already present leakage conduction path due to joule heating and to the high electric field,[50,51] while the oxygen species (O^{q-}) are drifted toward the bottom electrode, where they can easily diffuse along the TiN grain boundaries and can be stored. Once a filament is established in the HfO_2 layer, resulting in a significant variation of the layer resistance (R_3), most of the electric field will drop across the TiO_x, leading to a resistance change also in this layer. This finding is reported in literature for many bilayer structures,[28] and a thin layer of 2.5 nm of oxidized TiN was also reported to exhibit resistive switching properties.[52] The location of this additional filament portion depends on the TiO_x chemical, electrical, and morphological profile[53] and will be favored in correspondence of defective sites. In particular, the TiO_x layer is expected to exhibit a higher conductivity in correspondence of the former grain boundaries of the underlying TiN electrode,[54,55] which can efficiently exchange oxygen species and promote the filament formation. Therefore, the locally nonhomogeneous TiO_x interfacial layer provides preferential, nontrivial low resistance paths that allow lateral current flowing. Along the route of the maximum current, electrochemical processes are most likely to occur, leading to a switching in resistance for the series of resistors (R_2, R_1) connecting electrode A and the TiN bottom electrode.

After the set operation on device A, when the current is measured grounding electrode B (electrode A is floating), the reading current map (Figure 7b) displays an increase in conductivity also for device B. This latter finding can be explained by the current path passing through the common resistor R_1, whose resistance was changed during operation on device A. Conversely, other devices which did not show any relevant initial leaky current in the HfO_2, including the nearest neighboring cells of device A, remain insulated by a locally sturdy HfO_2 layer and do not show any relevant change in resistivity since the resistance R_4 dominates all the other resistances in the connecting network.

Finally, during the reset operation on device A, with the application of an opposite voltage polarity, the O^{q-} ions stored along the TiN grain boundaries diffuse upward and recombine with the V_O^{q+}, oxidizing the common lower portion of the filament and interrupting the conduction path for both the devices through an increase of resistance R_1.

The results of this work raise important questions about the real extension of the conductive filaments. Several direct experimental evidence in the HfO_2/TiN

film highlighted a spatial extension in the decananometers range.[12,56] Our data indicate that the presence of large grain boundaries in the oxidized TiN can extend the filament region even more. This consideration calls into question all the system scales in ultrahigh density arrays like the one we have being testing. Even if functional devices down to 10 nm have been demonstrated,[37] at the current stage it is impossible to exclude that the conductive filaments could extend beyond the limits of the single cell or that lateral sneak paths due to memory stack nonhomogeneities can cause a potential cross-talk issue in ultrahigh density memory arrays.

In our experiment, the cross-talk was observed between two devices already showing a certain degree of conduction in the initial state. If however we envisage to form all the devices in the array, the presence of sneak paths in the underlying film can become a severe issue, with two or more devices being influenced by an adjacent one in case of a low resistance path is established between neighboring devices as depicted in Figure 9. This phenomenon can arise whenever the spacing of the device array becomes comparable to the intrinsic defectivity length of the materials in the memory stack.

In conclusion, the observed effect is the result of localized leaky paths in the HfO_2 film in combination with a switching layer located at HfO_2/TiN interface, where the intrinsic defective and nonhomogeneous structure gives rise to lateral conduction along low resistance sneak paths.

The TiO_x which forms at the upper TiN interface is in general unavoidable, owing to the exposure to an oxygen-rich ambient and to the ALD deposition process. At the same time, the general features of the TiN film, including the polycrystalline morphology, are commonly encountered among different deposition techniques and are not limited to the sputter deposition method.[57] It is worth noting that the HfO_2/TiN stack is currently widely adopted among the best performing devices found in the literature, as both materials are very well integrated in the Si-based IC processes.[58]

The observed cross-talk is expected to occur in memory architectures in which a lateral physical connection exists between different devices. The integration of a continuous oxide film or electrode is however of crucial importance in many recent prototype applications of highly scaled ReRAM devices, based on both planar technology[33] or on a three-dimensional integration.[15,16,59] In the latter case in particular, the near proximity of the stacked cells make them particularly vulnerable to the cross-talk issue and it must be considered during the structure design. While the oxide/electrode patterning would provide a possible solution, it is responsible for a variety of additional issues related to the etching procedure and encapsulation,[14] and is hardly applicable in case of stacked integration of vertical ReRAM devices.

CONCLUSIONS

A bottom-up fabrication approach based on BCP self-assembling allowed the fabrication of an ordered array of Pt/Ti/HfO_2/TiN resistive switching memory devices with a well-controlled diameter of 28 nm and a density of 5×10^{10} devices/cm^2, with further device downscaling possible. The bilayer Pt/Ti top metal electrodes were contacted using C-AFM, allowing a characterization of the device initial state variability, which was correlated with the inherent presence of the leakage current paths randomly spread in the HfO_2/TiN stack. The bipolar RS operation was confirmed for the produced nanoscale devices, with a forming voltage lower than what is in general observed with the direct adoption of the C-AFM tip as top electrode. Because of the high density of the nanodevices under study, we observed a cross-talk between two different memory cells at a distance of 75 nm. We related the observed cross-talk phenomenon to the structure of the switching device, which determines the formation of filamentary conduction paths leading to sneak connections among different devices. Therefore, the reported experimental data suggest the occurrence of an important scalability issue for ultrahigh density memory arrays based on continuous HfO_2/TiN thin films. In particular, the latter approach, which has been suggested as a possible solution for the 3D integration of RS memory devices, fails when considering high density structures and consequently alternative integration schemes need to be envisioned in order to decouple the electrical switching phenomena of each single cell.

METHODS

Substrate Cleaning and Bottom Electrode Processing. n^{++} Si wafers (0.003−0.007 Ωcm) were cleaned by standard SC-2 (HCl:H_2O_2:H_2O 1:1:5 solution) cleaning procedure; the native oxide was removed by 10 s dip in HF solution (1:50), resulting in H-terminated Si. 10 nm Ti adhesion layer and 40 nm TiN as back electrode were afterward deposited by sputter deposition (100W RF power; 40 sccm Ar and 40 sccm Ar/4 sccm N_2 flux for the Ti and TiN depositions, respectively).

ALD HfO_2 Oxide Deposition. A 3 nm thick HfO_2 film was deposited on the bottom electrode by atomic layer deposition using Bis(methylcyclopentadienyl)methoxymethylhafnium(IV) (HfD-O4) and H_2O as precursors in the Savannah 200 ALD reactor (Cambridge Nanotech. Inc.) at 300 °C substrate temperature.[60,61] Film thickness and dielectric properties were monitored by spectroscopic ellipsometry (Woolliam, Inc.).

Brush Layer and Block Copolymer Deposition. Samples were sonicated in an isopropanol bath prior to polymer deposition to remove particles contamination. A hydroxyl-terminated

poly(styrene-r-methyl methacrylate) random copolymer with molecular weight M_n = 14 kg/mol, Styrene fraction *f* 0.62, and polydispersivity index PDI 1.09 in a toluene solution (9 mg in 1 mL) was spun at 3000 rpm for 30 s on the HfO_2 substrate for substrate neutralization and annealed at 310 °C for 10 min dwell time in an RTP machine (20 °C/s ramp) in N_2 ambient (1000 sccm). A 5 min toluene bath removed the ungrafted polymer chains. A film of polystyrene-*b*-poly(methyl methacrylate) BCP (Polymer Source Inc.) was afterward spun on the neutralized surface. A toluene solution (9 mg in 1 mL) was used (M_n 101.5 kg/mol, *f* 0.67, PDI 1.07), spun on the surface at 3000 rpm for 30 s, resulting in a film thickness of approximately 30 nm. The self-assembling was promoted with a 250 °C RTP annealing for 5 min in N_2 ambient. The final nanoporous PS template was obtained by removing the PMMA component with UV (5 mW/cm^2, λ 253.7 nm) for 15 min followed by a 100% acetic acid etch for 8 min, rinsing in water and drying in N_2 flow and a final oxygen plasma treatment at 40 W for a total of 130 s.

Images of the samples surface were acquired with a FE-SEM (Supra 40, Carl Zeiss) at 15 kV using the in-lens detector.

Top Electrodes Nanopatterning. A film of 4 nm Ti/6 nm Pt was deposited by electron-beam deposition on top of the nanoporous PS template, with a chamber pressure lower than 2×10^{-6} mbar. The lift-off process was carried out in warm toluene (80 °C, sonication bath).[19,62,63]

AFM Electrical and Morphological Characterization. A Dimension Edge instrument (Bruker) equipped with a TUNA electrometer (1 pA to 1 μA current range) was used in combination with highly doped diamond-coated tips (CDT-CONTR, nanosensor, with 100−200 nm curvature radius but a nanoroughness in the 10 nm regime, lowering the contact area) or Pt/Ir coated tips (PPP-CONTPt, nanosensor, with a 25 nm thick coating on top of a <10 nm curvature radius tip). The bias voltage was applied to the substrate, while the tip was held grounded.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Initial state conductance and device variability for two different sample areas; comparison between the distribution of leaky sites in the bare HfO_2 film and the density of the patterned devices; forming operations attempted using the Pt/Ir C-AFM tip as top electrode. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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